Claim Amendments

Please amend claims 1-3, 7, 10, 11, 13-15, 17, and 20 as follows:

Please cancel claims 4-6, 9, 12, and 16 as follows:

Please add new claims 21 - 26 as follows:

Claims as Amended

1. (currently amended) A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process~~, the method~~ comprising the steps of:

providing an inter-metal dielectric (IMD) layer ~~including~~ comprising at least one via opening extending ~~substantially perpendicular to~~ through a thickness ~~therethrough~~ thereof; ~~and,~~

~~conformally~~ forming an antireflectance coating (ARC) layer over ~~said~~ the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening ~~to reduce light reflectance~~ without filling the at least one via opening~~.~~; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

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2. (currently amended) The method according to claim 1, wherein ~~prior to the step of conformally forming an ARC layer~~ an etching stop layer is ~~formed~~ provided over said IMD layer~~, and a first antireflectance coating (ARC) layer~~ the ARC layer ~~is formed over said~~ the ~~etching stop layer~~.

3. (currently amended) The method of claim 2, wherein the etching stop layer ~~comprises~~ is selected from the group consisting of silicon oxynitride and silicon nitride.

4. cancelled

5. cancelled

6. cancelled

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7. (currently amended) The method of claim 1, wherein the ARC layer is selected from the group consisting of ~~at least one of~~ silicon oxynitride and titanium nitride.

8. (original) The method of claim 1, wherein the ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

9. cancelled

10. (currently amended) The method of claim 1, wherein ~~said~~ the at least one via opening includes at least two via openings formed substantially adjacent to one another.

11. (currently amended) A method of reducing a~~n~~ photoresist undercutting ~~effect~~ due to via sidewall light reflections in a dual damascene trench patterning process ~~in a photoresist layer in a photolithographic process~~ comprising the steps of:

providing an inter-metal dielectric (IMD) layer ~~further~~ comprising a first anti-reflectance coating (ARC) layer over the IMD layer;

forming via openings extending through a thickness portion ~~said~~ of the IMD layer;

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substantially conformally ~~forming~~ depositing ~~an anti-reflectance coating (ARC)~~ a second ARC layer over said IMD layer and ~~said~~ the via openings to cover the via opening sidewalls without filling the one via openings; and,

forming a photoresist layer over ~~said~~ the IMD layer and photolithographically ~~exposing a pattern defining~~ patterning trench openings disposed at least partially over ~~said~~ one or more of the via opening~~s~~.

12. cancelled

13. (currently amended) The method of claim 11, wherein ~~prior to forming the ARC layer,~~ an etching stop layer is ~~formed~~ provided over the IMD layer underlying the first ARC layer.

14. (currently amended) The method of claim 13, wherein the etching stop layer is selected from the group consisting of ~~comprises~~ silicon oxynitride and silicon nitride.

15. (currently amended) The method of claim 11, wherein the first and second ARC layers ~~is~~ are selected from the group consisting of ~~at least one of~~ silicon oxynitride and titanium nitride.

16. cancelled

A9 cont. 17. (currently amended) The method of claim 11, wherein the second ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

18. (original) The method of claim 11, wherein said via openings are formed substantially adjacent to one another.

19. (original) The method of claim 11, further comprising repeating said method as part of a manufacturing process to form a multi-level interconnected semiconductor structure.

20. (currently amended) An improved method of reducing light reflectance from via sidewalls in a dual damascene trench patterning process ~~structure, the method~~ comprising the steps of:

forming a first dielectric layer ~~on~~ over an underlying substrate;

forming at least one second dielectric layer over said first dielectric layer;

forming at least one anti-reflectance coating (ARC) layer over the at least one dielectric layer;

forming at least one via opening ~~substantially~~ through a thickness of the ARC layer, the at least one second dielectric layer, and the first dielectric layer;

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forming at least one additional ARC layer substantially conformally over the at least one ARC layer and the at least one via opening to cover the at least one via opening without filling the at least one via opening;

forming a layer of photoresist over the at least one additional ARC layer; and,

~~exposing selected regions of the layer of photoresist layer to light such that the light penetrates the layer of photoresist and is at least partially absorbed by the at least one additional ARC layer and the at least one ARC layer.~~

photolithographically patterning a trench opening over the at least one via opening.

21. (new) The method of claim 1, wherein the ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

22. (new) The method of claim 11, wherein at least the second ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

23. (new) The method of claim 1, wherein the ARC layer consists essentially of silicon oxynitride.

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24. (new) The method of claim 11, wherein the first and second ARC layers consist essentially of silicon oxynitride.

25. (new) The method of claim 1, further comprising forming a dual damascene structure.

26. (new) The method of claim 11, further comprising forming a dual damascene structure.